CIRCUIT DESIGNER'S NOTEBOOK

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KYOCERA
AVX®

CIRCUIT DESIGNER'S NOTEBOOK

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CAPACITOR DIELECTRIC PROPERTIES

Dielectric materials play a major role in determining the operating characteristics of ceramic chip capacitors. Accordingly, they are formulated to meet specific performance needs. The following definitions are provided as a general overview of pertinent dielectric design parameters.

Dielectric Constant: Also referred to as relative permitivity (ε_r), a dielectric property that determines the amount of electrostatic energy stored in a capacitor relative to a vacuum. The relationship between dielectric constant and capacitance in a multilayer capacitor can be calculated by, $C = \varepsilon_r$ (n-1) A/d, where ε_r is the dielectric constant, n is the number of electrodes, A is the active electrode area and d is the dielectric thickness.

Dielectric Strength: The dielectric's ability to safely withstand voltage stresses. This is determined primarily by the dielectric formulation and electrode spacing.
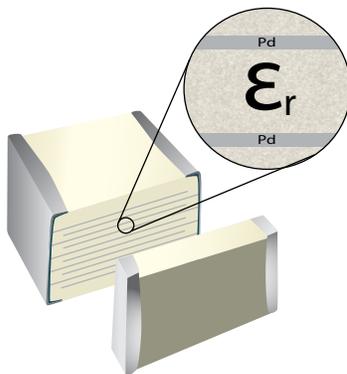
Excessive voltage gradients in ceramic capacitors will cause the dielectric to lose its insulating properties, resulting in catastrophic failure. The dielectric voltage breakdown characteristic is also affected by environmental conditions such as operating temperture, humidity, and atmospheric pressure as well as the physical spacing between the capacitor's terminations.

Internal breakdown: An internal failure condition that occurs when the applied voltage exceeds the dielectric strength, generally shorting the capacitor.

External breakdown: A failure condition that occurs when the applied voltage exceeds the breakdown path on the outside of the case between terminations.

Dielectric Thickness: This parameter defines the distance between any two internal electrodes after the ceramic has been sintered to its final state. This is a major factor in determining the voltage rating and parallel resonant frequency characteristics.
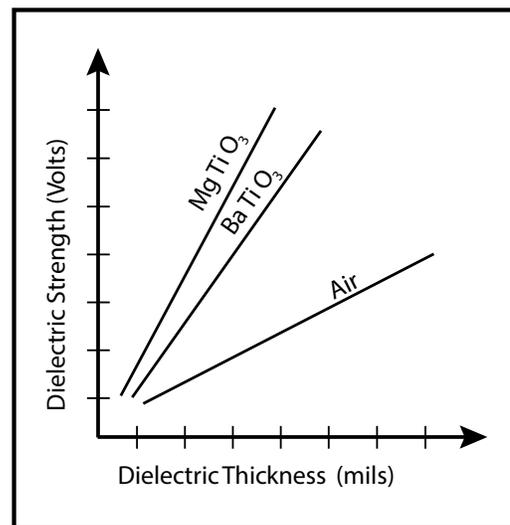
Dielectric Formulations: Formulations used in the design of ceramic capacitors are typically alkaline earth titanates, the most common of which is Barium Titanate ($BaTiO_3$). Electrical properties such as voltage rating, dissipation factor, insulation resistance, temperature coefficient, as well as dielectric constant, are determined by the dielectric formulation. These properties are tailored to specific applications through the addition of appropriate chemical modifiers such as alkaline earth elements and transition element oxides.
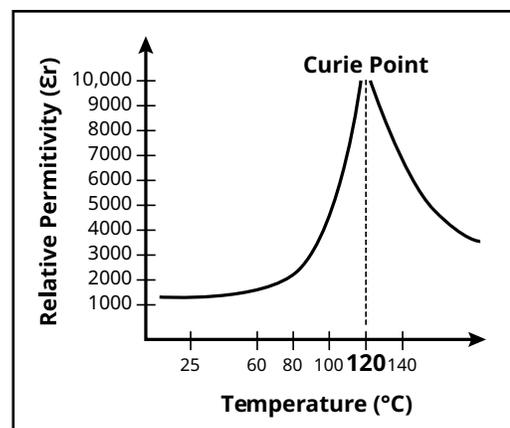
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CAPACITOR DIELECTRIC PROPERTIES

Curie Point: The temperature at which the ceramic material will exhibit a peak or sudden increase in dielectric constant is the Curie Point. Chemical agents may be added, to shift and/or depress the Curie Point. This is a major consideration in designing for specific Temperature Coefficient of Capacitance (TCC) limits.

Grain: A particle of ceramic material exhibiting a crystaline or polycrystaline structure. Electrical properties such as dielectric strength, dielectric constant, and voltage sensitivity are directly related to this parameter. Grain size also affects other electrical properties since it plays an important role in the formation of microstructural characteristics such as ceramic porosity and shrinkage related anomalies.

Temperature Coefficient of Capacitance (TCC): The maximum change of capacitance over the specified temperature range is governed by the specific dielectric material.

Insulation Resistance (IR): The DC resistance offered by the dielectric which is commonly measured by charging the capacitor to rated voltage for one minute and measuring the leakage current flow.

Dissipation Factor (DF): Denotes that portion of the total energy in the capacitor that is lost as internal heat or the ratio of energy dissipated to the energy stored.

Dielectric Aging: The gradual decrease of dielectric constant leading to loss of capacitance over time for certain ceramic formulations. This loss is logarithmic with time and is most pronounced shortly after manufacturing.

KYOCREA AVX's: Design Philosophy - KYOCREA AVX capacitors are designed and formulated in such a manner as to optimize all performance characteristics. As an example, using closely spaced electrodes, i.e., thin dielectric sections, will generally increase the parallel resonant frequency but will also decrease the maximum voltage rating. In this instance, dielectric spacing and active electrode overlap areas are balanced for the best combination for the specific application category. Another example may involve the inclusion of additives to adjust the TCC of a given dielectric class. This is accomplished by optimizing TCC while maintaining good insulation resistance and dissipation factor characteristics.

ESR LOSS FACTORS

The summation of all losses in a capacitor is called Equivalent Series Resistance, (ESR) and is typically expressed as milli-ohms. ESR losses are comprised of both dielectric loss (Rsd), and metal loss (Rsm).

$$ESR = Rsd + Rsm$$

Dielectric loss (Rsd) is determined by the specific characteristics of the dielectric material. Each dielectric material has an associated loss factor called loss tangent. The loss tangent is numerically equal to the dissipation factor (DF) and is a measure of loss in the capacitor's dielectric at RF frequencies. The effect of this loss will cause the dielectric to heat. In extreme cases thermal breakdown may lead to catastrophic failure. The dissipation factor (DF) provides a good indication of the dielectric loss, and is typically measured at low frequencies e.g. 1MHz, where this loss factor is predominant.

Metal loss (Rsm) is determined by the specific conductive properties of all metallic materials in the capacitor's construction. This includes electrodes, terminations plus any other metals such as barrier layers etc. The effect of Rsm will also cause heating of the capacitor. In extreme cases thermal breakdown may lead to catastrophic failure. These losses encompass ohmic losses as well as 'skin effect' losses at frequencies typically above 30 MHz for most MLCs.

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ESR LOSS FACTORS

Example:
Given a 100pF capacitor with an ESR of 18 milli-ohms (due to Rsm) @ 30 MHz, what is the ESR of this capacitor at 120 MHz?

Solution:
Take the square root of the ratio of the two frequencies

$\sqrt{120/30} = \sqrt{4} = 2$

Answer:
The ESR at 120 MHz is two times higher or 36 milli-ohms.

The following table illustrates the contribution of dielectric and metal losses for a 22pF 180R series capacitor. The losses are tabulated at various frequencies and are added together to yield ESR. Note that the dielectric losses are predominant at the lower frequencies and diminish at higher frequencies. The converse is also true for metal losses. Other capacitor values have the same pattern with different splits between Rsd and Rsm.

Catalog ESR curves typically denote ESR values for frequencies at or above 30 MHz, where the losses are predominantly due to Rsm. At these frequencies the dielectric losses are virtually transparent and do not significantly influence the overall ESR.

Frequency (MHz)	Capacitor (pF)	Rsd (m-ohm)	Rsm (m-ohm)	ESR (m-ohm)
1	180R220	145	7	152
3	180R220	48.2	7.8	56
30	180R220	4.82	9.18	14
300	180R220	0.48	28.51	29
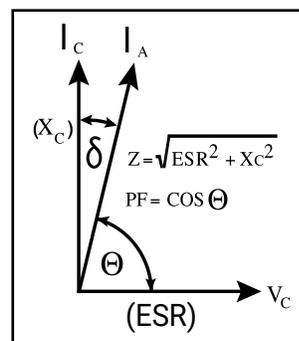
ESR =	Q =	DF =	X_c =
$X_c \times DF$	1/DF	1/Q	$1/2\,\pi \times F \times C$
X_c / Q	X_c / ESR	ESR/X_c	ESR/DF
$X_c \times \tan\delta$	$1/\tan\delta$	$\tan\delta$	$ESR \times Q$

Table 2: Relationship between ESR, Q, DF and X_c

In most instances it is important to consider ESR and Q for designs at high frequencies and DF for designs at lower frequencies. The general rule is that DF is a factor that will help the design engineer evaluate Rsd losses at low frequencies, usually well below 10 MHz, while ESR and the associated Q value are virtually always associated with Rsm losses at higher radio frequencies i.e. above 30 MHz through microwaves.

CAPACITOR ESR MEASUREMENT TECHNIQUE

Equivalent Series Resistance (ESR) is the summation of all losses resulting from dielectric (Rsd) and metal elements (Rsm) of the capacitor. Dielectric loss tangent of ceramic capacitors is dependant upon specific characteristics of the dielectric formulation, level of impurities, as well as microstructural factors such as grain size, morphology, and porosity (density). Metal losses are dependent on resistive characteristics of the electrode and termination materials, as well as the associated frequency dependent losses in electrodes due to skin effect. ESR is a key parameter to consider when utilizing capacitors in RF designs. A reliable and repeatable test method must be implemented in order to establish valid capacitor ESR characterizations.

Measurement Methodology:
Measuring the ESR of high Q ceramic chip capacitors requires a test system with an inherent Q higher than the device under test (DUT). A high Q coaxial resonant line is most commonly utilized for

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CAPACITOR ESR MEASUREMENT TECHNIQUE

these measurements. The coaxial line resonator is typically constructed from copper tubing and a solid copper rod for its center conductor. The DUT is placed in series between the center conductor and ground.

Before performing ESR measurements the unloaded characteristics of the resonant line must be established. This is accomplished by providing RF excitation to the shorted coaxial line and ascertaining the 1/4 and 3/4 lambda bandwidth. The line is then open circuited after which the 1/2 and 1 lambda bandwidth measurements are established. This data is used to characterize the unloaded Q of the resonant line, fixture resistance and resonant frequency. The unloaded Q of the line is typically in the order of 1300 to 5000 (130MHz to 3GHz) with a fixture resistance rfo in the range of 5 to 7 milliohms.

The capacitor sample is placed in series with a shorting plunger located at the low impedance end of the line. The generator is tuned for a peak resonant voltage, and then re-tuned to 6dB down from the peak voltage on both skirts of resonance. A loosely coupled RF millivoltmeter probe located at the high impedance end of the line (approximately at 1/4 wavelength from the shorted end) will measure RF voltage at the 6dB points.

The DUT perturbs the Q of the line changing the resonant frequency and bandwidth as compared to the unloaded line. The corresponding 6dB down frequencies referred to as fa and fb are used in the calculation of the capacitor's ESR. This process is referred to as the Q perturbation method. See Figure 1.

Note: Since the capacitive reactance of the test sample is in series with the line, it will shorten its electrical length depending on capacitor value. Values above 10pF will yield reasonable measurement accuracies however, as we approach 1pF the measured ESR may develop substantial errors. The small capacitance values exhibiting high X_C will cause the electrical length of the line to drastically change. The reactance of the line is equal and opposite to that of the DUT, at resonance.
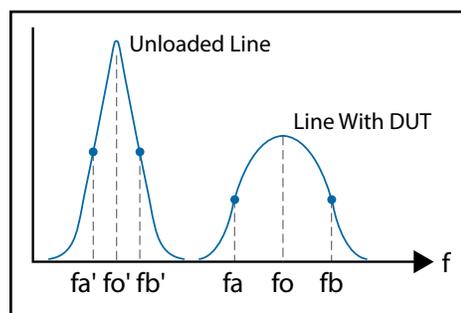
Figure 1: (Two Bandwidth Curves)

ESR Test System:

The test system most commonly used consists of a coaxial line (Boonton Model 34A) nominally (57.7cm) in length, with a resonant frequency of 130MHz and a characteristic impedance of 75 ohms. This impedance is chosen because it yields the highest line Q. Different line lengths may also be used for other frequency ranges.

A signal generator is connected to the low impedance end of the line and terminates in a non-inductive precision resistor. The resistor is mounted on a TNC connector and inserted into the DUT end of the line. It has an exposed loop that serves to loosely couple RF energy into the line. An RF excitation of 1 mw (0dBm) drives the shorted line through the source loop. The generator is swept until a peak resonant voltage is displayed on the RF millivoltmeter. The source loop is physically rotated until a 3 millivolt reference voltage is achieved at the high impedance end of the line. This procedure insures that the RF excitation does not load the line. See Figure 2.

An RF probe located at the high impedance end of the line is connected to a millivoltmeter to measure RF voltage at resonance. From these measurements the bandwidth and Q can be established. ESR is calculated by equating the change in bandwidth (BW) and Q, as compared to the initial unloaded shorted line condition. The BW data is put into an equation along with the initial line characterizations to calculate the ESR of the test sample. ESR measurements described here are performed in the series mode and can be achieved up to about 3 GHz.

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CAPACITOR ESR MEASUREMENT TECHNIQUE
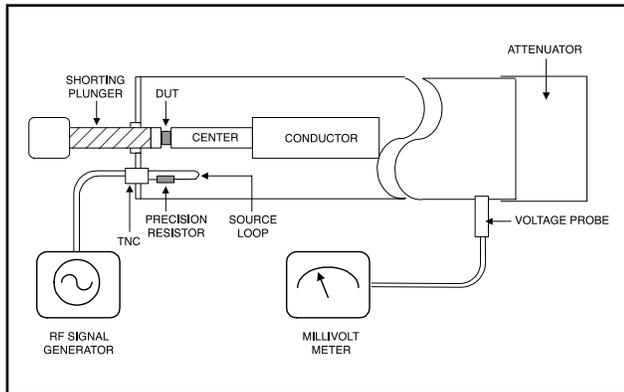
Figure 2: (Coaxial Resonator with DUT)

Factors Affecting ESR Measurement:
- Frequency measurement data for establishing BW require a minimum of four decimal places however, five places is desirable.
- Source and measurement probes must be loosely coupled to the line.
- The high impedance end of line should be shielded to reduce loss due to radiation to preserve Q. The shield is a cut-off attenuator offering 16DB attenuation per radius.
- Placement of the DUT in the line fixture should be consistent.
- Keeping fixture contact surfaces clean is essential for good repeatability.

UNDERSTANDING TEMPERATURE COEFFICIENT OF CAPACITANCE

Temperature Coefficient of Capacitance (TCC) describes the maximum change in capacitance over a specified temperature range. The capacitance value stated by the manufacturer is established at a reference temperature of 25°C. TCC should always be considered for applications operating above or below this temperature.

Class 1 Capacitors – These capacitors are highly stable with temperature and are referred to as temperature compensating. TCC specifications for class 1 capacitors will always specify the capacitance change in parts per million (ppm) per degrees centigrade. The maximum capacitance change is calculated by multiplying the capacitance by the TCC by the change in temperature above or below the reference temperature all divided by 1,000,000.

> **Example:** Given a 1000 pF NPO capacitor, what is the maximum capaictance drift at 35 °C?
>
> **Solution:** TCC for an NPO is 0±30 ppm per °C. Change in temperature from the 25 °C reference = 35 – 25 = 10 °C
>
> **Answer:**
>
> $$\frac{\text{cap value x TCC x } \Delta T}{1,000,000} = \text{cap change}$$
>
> **or**
>
> $$\frac{1000 \text{ pF x } \pm 30 \text{ (ppm) x } 10}{1,000,000} = \pm 0.3 \text{ pF}$$

Therefore, a 1000 pF capacitor subjected to a 10°C change in temperature may result in a value as high as 1000.3 pF or as low as 999.7 pF.

Class 1 capacitors are best suited for applications where stability over a wide variation of temperatures and high Q are required. Filter networks, and most circuits associated with tuning and timing as well as various types of resonant circuits generally require class 1 capacitors.

Class 2 Capacitors – Class 2 capacitors are not as temperature stable as class 1 however their main advantage is volumetric efficiency, i.e. more capacitance for a given case size. These capacitors are best suited for applications where higher capacitance values are important while Q and stability over temperature are not of major concern. TCC for class 2 capacitor dielectrics is expressed as a percentage.

The maximum capacitance change is therefore calculated by multiplying the specified capacitance by the percentage associated with the TCC for that capacitor.

> **Example:** Given a 1000 pF X7R capacitor, what is the maximum capacitance change?
>
> **Solution:** TCC for an X7R is ± 15%
> 1000 pF x 0.15 = 150 pF

UNDERSTANDING TEMPERATURE COEFFICIENT OF CAPACITANCE

Therefore in this example a 1000 pF capacitor at temperatures above or below 25°C reference may be as high as 1150 pF and as low as 850 pF.

EIA Class 2 TCC Designations

First Character: Defines the low temperature limit.
X = -55 °C   Y = -30 °C   Z = +10 °C

Second Character: Defines the high temperature limit.
5 = +85 °C   6 = +105 °C   7 = +125 °C

Third Character: Defines the maximum capacitance change in percentage.

V = +22, -82%	R = ±15%
U = +22, -56%	P = ±10%
T = +22, -33%	F = ±7.5%
S = ±22%	E = ±4.7%

Conclusion – TCC should always be factored in to designs operating at temperatures above or below 25°C. Further information on this topic can be obtained from the RF Applications department.

UNDERSTANDING INSULATION RESISTANCE

Insulation Resistance (IR) is a measure of the insulating property of dielectric materials and is typically expressed in meg-ohms. The insulation resistance includes both volume and surface resistance and can be expressed as the parallel combination of the two.

Insulation Resistance = RVxRS/(RV+RS)

Volume resistivity: R_v (ohms cm) also called bulk resistance represents the resistance per unit volume associated with a dielectric material.

Surface resistance: R_s (ohms/sq.) also called sheet resistance represents resist-ance per unit area and accounts for the leakage path on the outside surfaces of the capacitor. This is a material property; however, surface contamination and porosity also influence this parameter.

IR Measurements:
An IR meter is set up to measure insulation resist-ance by applying a voltage, typically equal to the capacitor's rated working voltage (WVDC), for about one minute. After the capacitor has been charged, the leakage current is then measured. The IR value is determined by taking the ratio of the applied dc voltage across the capacitor and the resultant leakage current after the initial charging period. This value is expressed as leakage or insulation resistance. A typical IR for a KYOCREA AVX porcelain chip capacitor is in the order of 10^{12} ohms at 25°C.

The figure represents a simplified circuit of an IR meter with a capacitor IR model depicted between the dotted lines. R_{L1} is placed in series with the dc source in order to limit the charging current to 50ma. In addition R_{L1} will limit the current in instances where the IR is very low or the test sample is shorted. R_{L2} is placed in series with the microammeter in order to calibrate the leakage current into the appropriate insulation resistance value. The bleeder resistor (R_B) is placed across the capacitor in order to discharge the test sample after the measurement has been performed.

Factors Affecting IR:
Dielectric material properties and processing play a major role in determining the IR characteristics of ceramic chip capacitors. Specific formulations as well as ceramic firing profiles are major factors that determine the insulation resistance. Microstructural defects such as voids, cracks, delaminations, and foreign materials are also associated with variations of insulation resistance. These defects are undesirable and require tight control of manufacturing processes to prevent their occurrence.

UNDERSTANDING INSULATION RESISTANCE

Insulation resistance is primarily influenced by ionic imbalances in the ceramic crystal structure creating charge carriers that become mobile in the presence of an electric field. Increased numbers of mobile charge carriers result in leakage current paths that degrade the IR. Charge carrier mobility also increases with temperature, hence leading to lower insulation resistance at elevated temperatures. At 125°C the IR will degrade approximately one order of magnitude. Capacitors from various manufacturing lots are frequently tested at the highest rated operating temperature to make it easier to uncover defects in the dielectric. Other factors that effect IR are listed below.

R_v - Dielectric volume resistance. R_s - Dielectric surface resistance.
R_{L1} - Source current limit resistor. R_{L2} - Capacitor calibration resistor.
R_B - Bleeder resistor. DUT - Device under test.
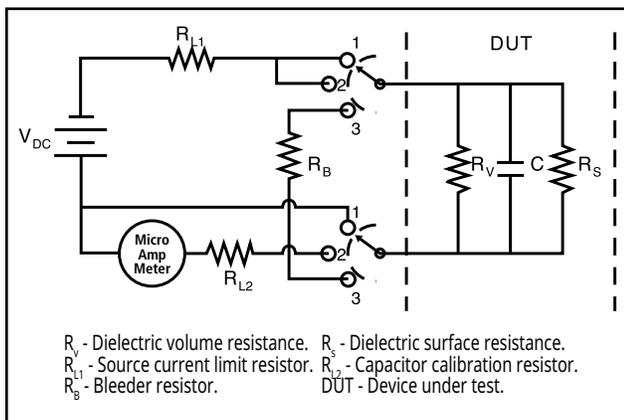
Schematic of IR meter with capacitor IR Model.

Additives: Chemical additives used in the dielectric formulation may exhibit a valence that will influence the IR of the dielectric. Care in selecting chemical additives such as various oxides must be exercised in order to optimize the IR.

Particle Size & Grain Boundaries: Small ceramic particle sizes will provide a fine grain structure in the ceramic. This is desirable because small grain sizes yield the greatest number of grain boundaries and will therefore act as a barrier to leakage current, thereby enhancing the IR.

Binder Systems: Used in the preparation of ceramic slurry and electrode paste and subsequently removed. This is accomplished during a slow heating cycle in which organic compounds are decomposed and eliminated. If the binders are not properly removed they may leave traces of carbon and other impurities in the ceramic. These residual

elements, reacting with the dielectric during sintering, may alter the distribution of mobile charge carriers and create conductive paths, thereby degrading the insulation resistance.

Impurities: Care must be taken throughout the manufacturing process to avoid process contamination. This condition can degrade the dielectric's IR property and therefore must be tightly controlled.

Surface Contamination: Solder flux, moisture, salts and any number of environmental contaminants can easily degrade the capacitor's insulation resistance. Care must be taken to clean the surface free of foreign materials.

Density/Porosity: Ceramic dielectrics must be manufactured as close to the theoretical density of the dielectric material as possible to minimize pores in the ceramic. Large pores in the ceramic microstructure can absorb environmental contaminants as well as moisture leading to degraded IR. This effect is most evident under high operating humidity and can be temporarily reversed by heating the capacitor, thereby baking out the moisture.

Application Considerations:
• Low IR can alter the bias condition of an FET amplifier by offering additional shunt resistance in the bias network.
• Capacitors used in dc blocking and coupling applications need to exhibit high IR to prevent dc leakage current from flowing.
• Filter and matching applications require high IR so that the overall circuit Q remains unaffected.
• The capacitors low frequency dissipation factor (DF) can be affected by low IR. This will make IR appear as a significant part of the dielectric loss, thereby degrading the DF. This degradation occurs because IR appears as a shunt resistance in parallel with the capacitor.
• Low IR in a high power bypass application may result in excessive heat dissipation and degraded circuit performance.
• Overall circuit performance and reliability may be affected over time by voltage stresses and elevated operating tempera-tures if the IR is initially degraded.

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DIELECTRIC AGING PHENOMENA

Dielectric Aging:

A capacitor's aging characteristic is an important consideration during manufacturing as well as in the end application. Appropriate allowances for this effect must be judiciously accounted for throughout the useful life of the product. This phenomenon is sometimes not regarded by the end user as being critical and can easily lead to circuit performance anomalies.

The term "capacitor aging" describes an effect exhibited by ferroelectric class dielectric materials in which barium titanate ($BaTiO_3$) is the main constituent. A decay in dielectric permittivity, epsilon (ε), is noted over time with these formulations. The aging rate defines an incremental downward change in dielectric permittivity and progresses logarithmically with time. Dielectric aging is typically expressed as a percent per decade hour, i.e., 1-10 hours, 10-100 hours, 100-1000 hours etc.

Dielectric aging is a result of relaxation of the crystalline microstructure of ferroelectric ceramic materials and is initially observed after sintering during room temperature stabilization. Capacitors fabricated with these dielectric materials will exhibit a rapid loss in capacitance value at first, and much more slowly thereafter.

Thus, a change in the dielectric constant, with time is observed during this relaxation period. The dielectric aging phenomena occurs predominantly in ferroelectric ceramic materials and is more prominent with formulations exhibiting high dielectric constants, i.e. EIA class 2 and 3. Therefore, aging rates tend to be somewhat proportional to the dielectric constant or permittivity of a given material. Refer to Table 1 and the example in Figure 1.

Dielectric	Typical Dielectric Constant	Typical Aging Rate
NPO	65	None
X7R	2,000	1.5% - 2.5%
BX	4,000	3% - 4%
Z5U	8,000	4% - 5%
Y5V	10,000	6% - 7%

Table 1: Aging Rates of various EIA Dielectrics.

Note: These are typical aging rates however variations from one commercial formulation to the next may vary significantly.
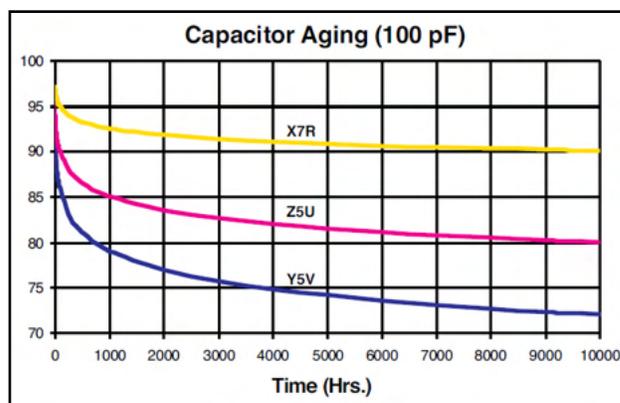
Figure 1: Example of Capacitor Aging – (100pF with various dielectric types).

Curie Temperature:

The Curie temperature is defined, as the point at which an alteration of the crystalline morphology occurs. The crystal structure changes from its initial tetragonal, non-symmetrical configuration below the Curie temperature, to a cubic perovskite symmetrical configuration above the Curie temperature. A sharp increase in dielectric constant (e) occurs at this temperature. This change in crystalline structure is typical for barium titanate ($BaTiO_3$) formulations and will exhibit a Curie temperature of 120°C. It is interesting to note that the Curie point can be shifted to a higher temperature and or its peak depressed through modifications of the ceramic formulation. Either of these modifications can be produced by the addition of specific additives.

Time zero on the dielectric aging clock starts with the last temperature treatment or heating cycle that exceeds the Curie temperature. This will include various stages in the manufacturing process such as binder burn out, termination, plating, and sintering each of which impose heating the ceramic material above the Curie temperature.

The capacitance is measured approximately 24 hours after chip fabrication, and likewise must be checked again 24 hours subsequent to each heating cycle. This procedure is performed to insure that when the user gets the part, it will

DIELECTRIC AGING PHENOMENA

have aged sufficiently so that the relative change in capacitance value is reasonably low. Over long periods of time, aging may cause capacitance to drift out of the specified tolerance on the low side. This loss of dielectric constant with time is unavoidable with ferroelectric materials, however it may be restored by re-heating the capacitor. The industry's standard procedure for de-aging a ceramic capacitor is to re-heat the capacitor to a temperature above the Curie point, typically 150°C, for about one hour. This will restore the capacitance back to the original high value at time to. Capacitor manufacturers ship parts so they will be well within tolerance after about ten days of aging.
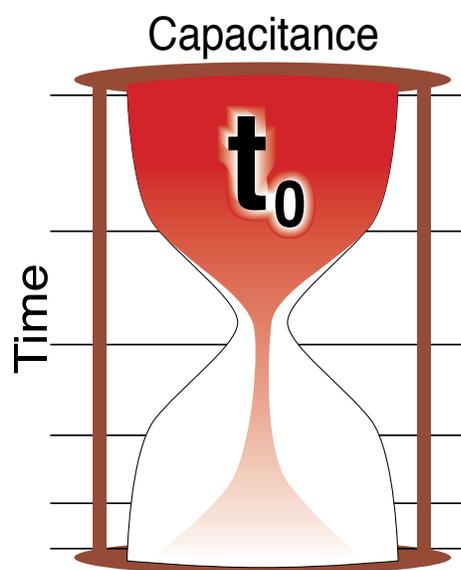
Capacitance / Time

Calculating Aging Rate:
The following formula gives the relationship between the aging rate and the capacitance after time t (hours). CA is the capacitance you can expect after a given time interval. C1 is arbitrarily chosen as 1 hour for the purpose of this example but is more commonly given as 24 hours and denotes the initialized capacitance value at time t0.

$$CA = C1\ (1 - A/100\ \text{Log}_{10}\ t)$$

Where: CA = Capacitance after t (hours)
    C1 = Capacitance at time t0
    A = Dielectric Aging Constant, (aging rate in percent)
    t = Time from Last Heating in hours

Application Considerations:
Select capacitors with low or no aging rates especially when designing minimum drift applications such as filters, tuning, matching and timing circuits.

Do not specify tight capacitance tolerances when designing ferroelectric class high K capacitors into an application. These capacitors can easily drift out of tolerance over time.

Evaluate the minimum required capacitance taking aging rate as well as temperature coefficient of capacitance (TCC) into account before designing ferroelectric devices into the circuit. This will many times require the designer to specify a guaranteed minimum value (GMV).

PIEZOELECTRIC EFFECT IN CERAMIC CAPACITORS

The Greek root of the word piezo means "to press". In 1880, Jacques and Pierre Curie discovered that pressure applied to a quartz crystal creates an electrical potential on the crystal. Likewise, they also discovered that an electrical potential impressed on the crystal creates a deformation of the crystal. They referred to this phenomenon as the piezoelectric effect.

The piezoelectric effect can be readily defined as the generation of an electrical potential as a result of applying pressure or by mechanically deforming

a piezo crystal lattice structure. This deformation causes the molecules in the material to become electrical generating dipoles resulting in a potential difference across the crystal.

The piezoelectric effect occurs in crystals that have no center of symmetry. This lends itself to a net polarization of the crystal. The most widely known piezoelectric material is quartz. Others include various polycrystalline ceramics that are frequently used in capacitor dielectric formulations. One such group of materials is **11**

PIEZOELECTRIC EFFECT IN CERAMIC CAPACITORS

known as perovskites. Perovskites are one of the most abundant minerals on earth and are used in a large family of crystalline ceramic formulations such as barium titanate, calcium titanite and lead zirconate titanate. These crystals have some inherent piezoelectric properties that require careful processing to minimize the piezoelectric effect when used in capacitor fabrication.

Ba O$_2$ Ti
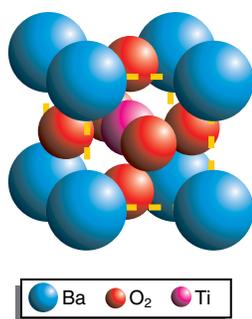
Example of a Perovskite Ceramic - Barium Titanate (BaTiO3)

Piezoelectric Ceramics:
Because of the anisotropic nature of many ceramics materials, piezoelectric effects are dependent on direction of mechanical excitation. This concept is illustrated by the ceramic element shown in the following figure. The axes labeled x, y, and z follow the classical right hand orthogonal axial set. The orthogonal coordinate system shown here is commonly used to describe piezoelectric properties. The reference direction is conventionally chosen as the z axis. A mechanical or electrical response in any of the three directions will produce a response in its corresponding orthogonal axis. For example, an electric field in the z direction causes a mechanical deformation in the x direction, and conversely a mechanical deformation in the x direction will result in an electric field in the z direction. The piezoelectric effect along any axis is dependent on a mechanical excitation of an orthogonal axis.
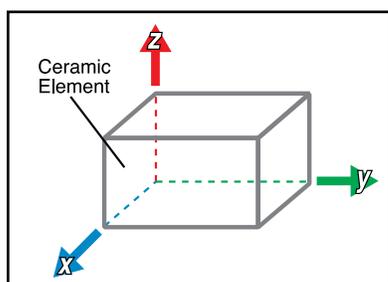
Circuit Application Considerations:
Stability: Issues regarding the generation of microphonics due to the piezoelectric effect can lead to a myriad of performance issues in many circuit applications.

Some examples are:
• Production of extraneous (unwanted) signal voltages due to structure borne vibration that can de-tune high Q circuits.
• Oscillator instability, especially where tuning is accomplished with passive components.
• Ringing in pulsed circuit applications.
• Generation of erroneous data in digital circuits.

Mechanical Stress:
Mechanical stress on the capacitor due to vibration can disrupt the termination-ceramic interface. The shear forces that exist in piezoelectric ceramics can lead to unreliable ceramic-termination interface. This condition may gradually reduce performance by progressively degrading the loss tangent (DF).

When RF voltage is applied to the capacitor, the microstructure will grow and shrink at the same frequency as that of the applied voltage. This can lead to shear forces that can cause deformations leading to reduced reliability or catastrophic failure.

Phase Sensitive Applications:
Capacitors exhibiting piezoelectric effects should not be used in filter network designs. Phase shifters, filters, oscillators, or any design where phase stability is essential, should avoid the application of piezoelectric dielectric materials, because phase variations in accordance with the mechanical excitation may occur.

Coupling Applications:
Interstage coupling applications are frequently sensitive to capacitors exhibiting piezoelectric effect. The designer should avoid using these capacitors in sensitive applications as they can pass along non-linear distortions to succeeding stages.

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EFFECTIVE CAPACITANCE VS FREQUENCY

It is generally assumed that the capacitance value selected from a vendor's catalog is constant over frequency. This is essentially true for applications with applied frequencies that are well below the capacitors self-resonant frequency. However as the operating frequency approaches the capacitors self-resonant frequency, the capacitance value will appear to increase resulting in an effective capacitance (C_E) that is larger than the nominal capacitance. This article will address the details of effective capacitance as a function of the application operating frequency. In order to illustrate this phenomenon, a simplified lumped element model of a capacitor connected to a frequency source operating in a network will be considered, as depicted in Figure 1.
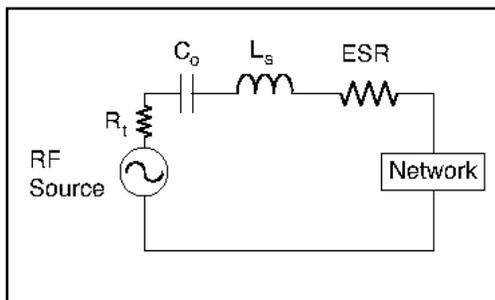
Figure 1: Lumped Element Equivalent Model

This model has been selected because the effective capacitance is largely a function of the net reactance developed between the capacitor and its parasitic series inductance (L_S). The equivalent series resistance 'ESR' shown in this illustration does not have a significant effect on the effective capacitance.

Effective Capacitance:

The nominal capacitance value (C_O) is established by a measurement performed at 1MHz. In typical RF applications the applied frequency is generally much higher than the 1MHz measurement frequency, hence at these frequencies the inductive reactance (X_L) associated with the parasitic series inductance (L_S) becomes significantly large as compared to the capacitive reactance (X_C). Figure 2 illustrates that there is a disproportionate increase in X_L as compared to X_C with increasing frequencies. This results in an effective capacitance that is greater than the nominal capacitance. Finally at the capacitors series resonant frequency the two

reactance's are equal and opposite yielding a net reactance of zero. The expression for C_E becomes undefined at this frequency.
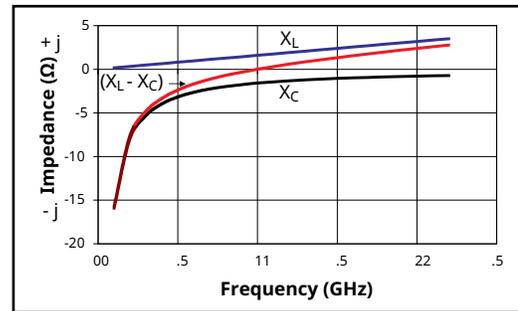
Figure 2: Net Impedance vs. Frequency

As illustrated in Figure 1, the physical capacitor can be represented as C_O in series with L_S. The impedance of the series combination of C_O and Lscan then be set equal to C_E, which may be referred to as an "ideal equivalent" capacitor. This will yield the following equation:

This will yield the following equation:

$$j\,(\omega\,L_S - 1/\omega\,C_0) = -\,j\,1/\omega\,C_E$$
$$\omega^2\,L_S - 1/C_0 = -\,1/C_E$$

The relationship between the operating frequency F0 and the effective capacitance CE can then be stated as:

$$C_E = C_0/(1 - \omega^2\,L_S\,C_0)$$
$$C_E = C_0/[1 - (2\pi\,F_0)^2\,L_S\,C_0]$$

Where:

C_E = Effective Capacitance at the application frequency, (F_0)

C_0 = Nominal Capacitance at 1 MHz

L_S = Parasitic Inductance, (H)

F_0 = Operating Frequency, (Hz)
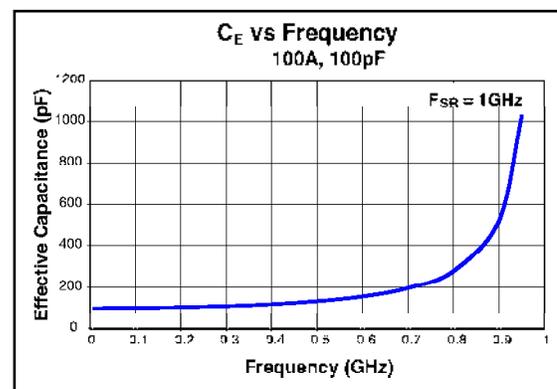
Figure 3: Effective Capacitance (C_E) vs. Frequency   **13**

EFFECTIVE CAPACITANCE VS FREQUENCY

From this relationship it can be seen that as the applied frequency increases the denominator becomes smaller thereby yielding a larger effective capacitance. At the capacitors series resonant frequency the denominator goes to zero and the expression becomes undefined. The relationship of C_E vs frequency is a hyperbolic function as illustrated in Figure 3.

Example:
Consider an 100A series 100pF capacitor.
Calculate the effective capacitance (C_E) at 10MHz, 100MHz, 500MHz, 900MHz, 950MHz.
Solution: Calculate by using the relationship $C_E = C_O/[1-(2\varpi F_O)2 L_S C_O]$. Refer to Table 1.

Operating Frequency	Effective Capacitance (C_E), pF	Impedance, (Ω)
10	100.01	0.013 – j 159.13
100	101.01	0.023 – j 15.76
500	133.34	0.051 – j 2.38
900	526.29	0.069 – j 0.337
950	1025.53	0.070 – j 0.168

Table 1: Relationship between F_0, C_E and Z

Application Considerations:
Impedance matching and minimum drift applications such as filters and oscillators require special attention regarding C_E. For applications below the capacitors self-resonant frequency the net impedance will be capacitive (-j) whereas for applied frequencies above resonance the net impedance will be inductive (+j). Operating above series resonance will correspondingly place the impedance of the capacitor on the inductive side of the Smith chart (+j). When designing for these applications both C_E and the sign of the net impedance at the operating frequency must be carefully considered.

In contrast, the majority of coupling, bypass and DC blocking applications are usually not sensitive to the sign of the impedance and can be capacitive or inductive, as long as the magnitude of the impedance is low at the applied frequency. The effective capacitance will be very large and the net impedance will be very low when operating close to resonance. At resonance the net impedance will be equal the magnitude of ESR and the capacitance will be undefined.

CAPACITORS IN COUPLING AND DC BLOCKING APPLICATIONS

Capacitors used in coupling and dc blocking applications serve to couple RF energy from one part of a circuit to another and are implemented as series elements. Proper selection of coupling capacitors insures the maximum transfer of RF energy. All capacitors will block dc by definition; however, considerations for satisfying the requirements of a coupling application depend on various frequency-dependent parameters that must be taken into account beforehand.

Figure 1 illustrates two RF amplifier stages operating in a 50-ohm network inter-connected by coupling capacitor C_0. Table 1 outlines several device options for achieving interstage coupling at various wireless frequencies. Electrical parameters such as series resonance, impedance, insertion loss, and equivalent series resistance must be evaluated in order to achieve an optimal coupling solution.
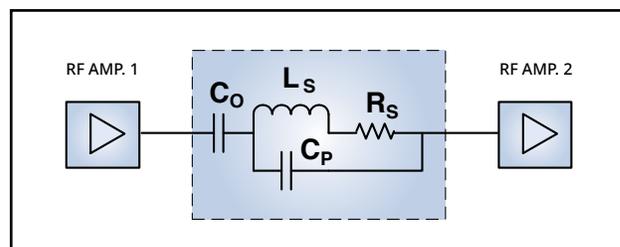
Figure 1: Interstage coupling block diagram

Note: Coupling capacitor C_0 in Figure 1 is represented with its equivalent series resistance (ESR) denoted as R_S, equivalent series inductance (ESL) denoted as L_S and parasitic parallel capacitance C_P, associated with the parallel resonant frequency (F_{PR}).

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CAPACITORS IN COUPLING AND DC BLOCKING APPLICATIONS

Frequency (MHz)	Device Options	FSR (MHz)	Insertion Loss S21 (dB)	ESR (ohms)	Package Size
900	100A101 – 100 pF	1000	< 0.1	0.072	55 mil x 55 mil
	600S101 – 100 pF	1340	< 0.1	0.070	0603
1900	100A270 – 27 pF	1870	< 0.1	0.161	55 mil x 55 mil
	600S560 – 56 pF	1890	< 0.1	0.085	0603
2400	100A160 – 16 pF	2410	< 0.1	0.218	55 mil x 55 mil
	600S390 – 39 pF	2340	< 0.1	0.140	0603

Table 1: Examples of coupling capacitors & associated parameters

A capacitor's series resonant frequency (F_{SR}) also referred to as self-resonance, occurs at

$$F_{SR} = \frac{1}{2\Pi \sqrt{L_s C_o}}$$

At this frequency the capacitor's net reactance is zero and the impedance is equal to the ESR. As shown in Table 1, a 100A101, (100 pF) porcelain capacitor has an FSR of 1000 MHz with a corresponding ESR of 0.072 ohms. At this frequency the capacitor will provide its lowest impedance path required for optimal coupling. In contrast the impedance of a capacitor at its parallel resonant frequency (F_{PR}) can be precipitously high. By assessing the magnitude of S21 vs. frequency for a given capacitor, excessive losses associated with F_{PR} at the operating frequency can be readily observed. In coupling applications a capacitor's F_{SR} can usually be exceeded without posing a problem as long as the net impedance remains low.

Net Impedance
The magnitude of a capacitor's impedance is equal to

$$\sqrt{(ESR)^2 + (X_L - X_C)^2}$$

As seen by this relationship a capacitor's impedance is significantly influenced by its net reactance ($X_C - X_L$). It is important to know the magnitude of the impedance throughout the desired passband. A properly selected coupling capacitor will exhibit suitably low impedance at these frequencies.

As seen in Figure 2 the net impedance below F_{SR} is capacitive and is dominated by $1/\omega C$ yielding
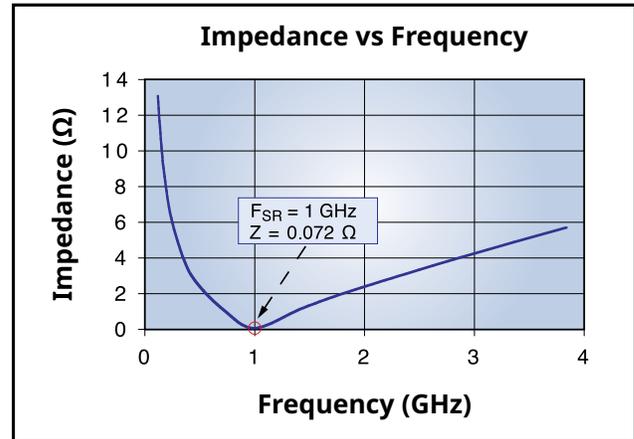
Figure 2: Impedance vs. Frequency for 100A101 (100pF)

a hyperbolic curve for frequencies less than F_{SR}. Conversely, the net impedance above F_{SR} is inductive and is dominated by ωL yielding a linear line segment for frequencies greater than F_{SR}.

Insertion Loss (S21)
One of the fundamental considerations for all coupling applications is the capacitor's insertion loss at the operating frequency. By eval-uating the magnitude of S21 the designer can readily determine whether or not the subject capacitor is suitable. It is especially important to look for the presence of one or more parallel resonances falling within the operating passband. These resonances will generally show up as distinct attenuation notches at their frequencies of occurrence. If a parallel resonance does fall within the operating passband it will be necessary to evaluate its depth in order to determine whether or not the loss is acceptable. In many instances the magnitude of S21 for a given capacitor may be excessive, rendering it unusable for the application. An insertion loss of several tenths of a dB is generally an acceptable criterion for most coupling applications. Losses that exceed several tenths of a dB within the passband could easily compromise the end performance of a circuit design. Therefore the decision is ultimately left up to the discretion of the designer to determine whether or not these losses are acceptable for a particular design requirement.

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CAPACITORS IN COUPLING AND DC BLOCKING APPLICATIONS

Insertion Loss (S21) - 100 pF
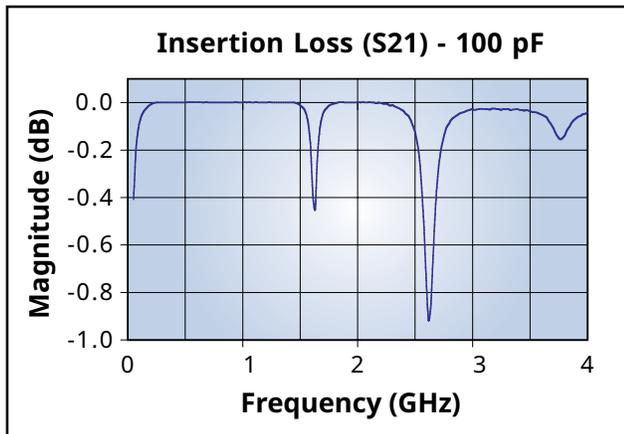
Figure 3: Insertion loss vs. Frequency for 100A101, 100 pF chip capacitor in flat mount orientation

Figure 3 illustrates the insertion loss characteristic of a 100A101 (100pF) capacitor. The sample was measured in a series through configuration from 50 MHz to 4 GHz with the capacitor's electrodes parallel to the substrate, i.e. flat mount orientation. As seen in Figure 3 the capacitor's insertion loss is less than 0.1 dB between 200 MHz to 1.5 GHz. By edge mounting the capacitor, i.e. electrodes perpendicular to the substrate, the first parallel resonant notch at 1.6 GHz will be suppressed. As a result the usable frequency range will be extended to approximately 2.4 GHz. In this orientation the same capacitor can be used to include all of the wireless frequencies in a broadband coupling application.

ESR and Q

A capacitor's quality factor (Q) is numerically equal to the ratio of its net reactance (XC – XL) to its equivalent series resistance

$$Q = \frac{|X_C - X_L|}{ESR}$$

From this expression it can be seen that the capacitor's Q varies inversely to its ESR and directly with the net reactance. A capacitor's ESR should be known at all frequencies within the passband, especially at frequencies above the capacitor's series resonant frequency. At the frequency where the electrode thickness is at least one skin depth the ESR will increase as the $\sqrt{f}$. Accordingly, the ESR will increase in this fashion for increasing frequencies and may become the dominant loss factor. As previously mentioned an attenuation notch will occur at the capacitor's F_{PR}, the depth of which is inversely proportional to the ESR. Therefore the capacitor's ESR will largely determine the depth of the attenuation notch at the parallel resonant frequency.

CAPACITORS IN BYPASS APPLICATIONS

Capacitors used in bypass applications are implemented as shunt elements and serve to carry RF energy from a specific point in the circuit to ground. Proper selection of a bypass capacitor will provide a very low impedance path to ground. In theory the ideal impedance is zero ohms; however a real capacitor will exhibit some impedance due to its reactance and inherent parasitic elements. Satisfying capacitive bypass application requirements entails careful analysis of various frequency dependent capacitor parameters such as series resonant frequency (F_{SR}), equivalent series resistance (ESR), and the magnitude of the impedance. The ESR and impedance should always be evaluated at the operating frequency.

Figure 1 is a block diagram illustrating a capacitor bypass application. Capacitor C_0 in this figure is represented with its equivalent series resistance denoted as R_S, equivalent series inductance (ESL) denoted as L_S and parasitic parallel capacitance C_P, associated with the parallel resonant frequency (F_{PR}).
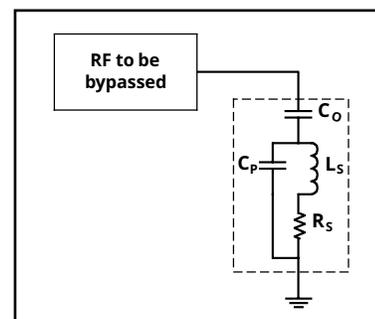
Figure 1: Bypass Capacitor Configuration

CAPACITORS IN BYPASS APPLICATIONS

Terminology:

Equivalent Series Resistance (ESR): Is the summation of all losses resulting from the dielectric (R_{SD}) and metal elements (R_{SM}) of a capacitor (R_{SD} + R_{SM}) and is typically expressed as milli-ohms. R_{SD} is the dielectric loss tangent and is dependent upon specific characteristics of the dielectric formulation and processing. Metal losses are dependent on resistive characteristics of the electrode and termination materials, as well as the losses of the electrodes due to skin effect. ESR is a key parameter to consider when utilizing capacitors in RF bypass applications.

Quality factor (Q): A capacitor's Q is numerically equal to the ratio of its net reactance (X_C - X_L) to its equivalent series resistance (ESR) or $Q = |X_C - X_L| / ESR$. From this expression it can be seen that the capacitor's Q varies inversely to its ESR and directly with its net reactance.

Series Resonant Frequency (F_{SR}): A resonance that occurs at $F_{SR} = 1/2\pi \sqrt{L_S C_O}$. At this frequency the capacitor's net reactance is zero and the impedance is equal to the ESR. The capacitor will provide its lowest impedance path required for optimal bypassing at this frequency.

Parallel Resonant Frequency (F_{PR}): A resonance occurring at approximately twice the F_{SR} for a parallel plate capacitor. In contrast to F_{SR} the impedance of a capacitor at its F_{PR} can be precipitously high. This is readily observed by assessing the magnitude of the insertion loss at F_{PR}.

Impedance: (Z) The magnitude of a capacitor's impedance is equal to $\sqrt{(ESR)^2 + (X_L - X_C)^2}$. As seen by this relationship a capacitor's impedance is significantly influenced by its net reactance (X_L-X_C).

It is important to evaluate the magnitude of the impedance throughout the desired frequency range. A properly selected bypass capacitor will exhibit suitably low impedance over this range. As seen in Figure 2 the net impedance below F_{SR} is capacitive and is dominated by $1/\omega C$, yielding a hyperbolic curve for frequencies less than F_{SR}. Conversely, the net impedance above F_{SR} is inductive and is dominated by ωL yielding a linear line segment for frequencies greater than F_{SR}.
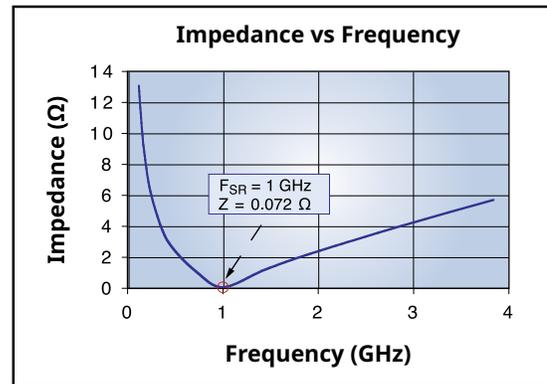
Figure 2: Impedance vs. Frequency for 100A101 (100pF)

Application Example

Bypassing is a critical design matter that requires careful consideration. Figure 3 shows a 1.9 GHz cellular FET amplifier with emphasis on the drain bias network.
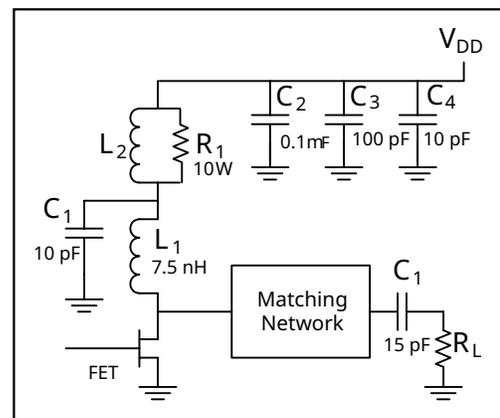
Figure 3: Bypass Capacitors in a 1.9GHz FET Broadband Bias Network

The circuit elements depicted in this figure will serve to suppress RF energy from getting onto the V_{DD} supply line while providing high impedance at the drain in order to maintain optimum in-band RF gain. It also functions to keep noise generated by the power supply from appearing on the drain of the FET. High-speed switching environments created by switch mode power supplies (SMPS) will generate noise on V_{DD} supply lines. Instantaneous current generated by fast rising and falling switch pulse edges can easily cause the V_{DD} supply line to ring. The resultant noise can include frequencies of up to several hundred megahertz. RF noise generated by SMPS switching is continuous and will generally occur up to frequencies equal to **17**

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CAPACITORS IN BYPASS APPLICATIONS

0.35 / P_E, where P_E = pulse rise or fall time (sec). For example a switched pulse with a rise and fall time of 1.5 ns will yield spurious spectral components up to 233 MHz.

Drain Bias Network:
As illustrated in Figure 3, the FET's drain bias network consists of series inductive elements having an impedance of ωL and shunt capacitive elements with an impedance of $1/\omega C$. Proper selection of bypass capacitors in the bias network is essential as they will serve to de-couple RF energy from the V_{DD} supply line to ground over a wide range of frequencies. Since capacitors exhibit a small parasitic inductance there is an associated series (self) resonant frequency where $F_{SR} = 1/2\pi \sqrt{L_sC_o}$. At F_{SR} the magnitude of the inductive and capacitive reactances are equal and hence the net impedance= $\sqrt{(ESR)^2 + (X_L - X_c)^2}$ is equal to a small ESR value. Accordingly the designer will ideally select a capacitor that has an F_{SR} at or close to the desired "bypass frequency". This preference is based on establishing a low impedance path with minimal or zero net reactance thereby making it ideal for bypassing applications.

F_{PR} usually occurs at more than twice F_{SR} for most multi-layer ceramic capacitors. At the capacitor's F_{PR}, the impedance is likely to be high and inductive (R+j ωL) and may not provide an adequate RF path to ground. To alleviate this, several capacitors are selected such that their self-resonant frequencies are staggered in order to cover a wide range of frequencies with reasonably low loss. The number of required capacitive elements depends on the loss and impedance characteristics of each element over the intended frequency band segments.

The inductors are in series with the drain and are not directly connected to reference RF ground. Accordingly they rely on bypass capacitors, C_1 through C_4 to achieve a low impedance path to ground. The combination of L_1 and C_1 will greatly suppress the in-band 1.9 GHz carrier frequency energy from appearing on the V_{DD} supply line. Inductor L_1 will act as a block at this frequency while capacitor C_1 will serve to further suppress in-band RF energy by bypassing it to ground. L_2 C_2, C_3 and C_4 will suppress RF energy at frequencies below the 1.9 GHz carrier frequency where the gain of the amplifier may be much higher. C_1's capacitance value is selected such that its F_{SR} is close to the amplifiers operating frequency. Since C_1 is a shunt element, and the impedance is low at its F_{SR}, the RF energy at the operating frequency will be bypassed to ground. Capacitor elements C_2, C_3 and C_4 are staggered in value and selected so that the impedance of each will be low at successive frequency segments in order to offer continuous bypassing of frequencies below the amplifier's operating band.

HIGH Q CAPACITORS IN MATCHING APPLICATIONS

Capacitor Q is almost always a primary design consideration in RF matching applications. The capacitor's power dissipation is inversely proportional to its Q factor and directly proportional to the equivalent series resistance (ESR). An input matching network is essential for most RF amplifier designs in order to transform the relatively low impedance of the active gain device to the system impedance. The active device's input impedance is typically in the order of 0.5 to 2 ohms and is generally matched to a 50 ohm system. Lets assume that a transistor in a power amplifier has an input impedance of 1 ohm. This will require an impedance transformation of 50:1. Therefore, we must trade off voltage for current as the matching network transforms the signal impedance from 50 ohms to 1 ohm. This will result in circulating current (i_3) to be more than seven times I_{IN}. See Figure 1.
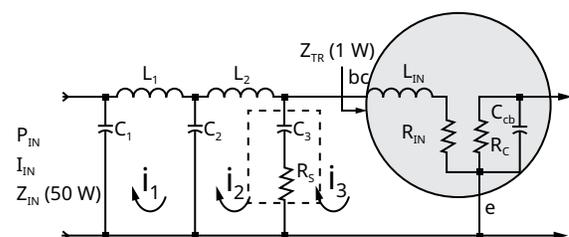
Figure 1: Capacitor Power Dissipation, Pd $= i^2 (X_c/Q)$ or $i^2 (ESR)$.   **18**

CIRCUIT DESIGNER'S NOTEBOOK

HIGH Q CAPACITORS IN MATCHING APPLICATIONS

Reasons for designing High Q capacitors into matching networks:

Output Capability – Low loss High Q capacitors in matching network applications will insure maximum effective gain and available output of the amplifier. Losses due to component heating especially in high RF power applications are greatly alleviated with the use of high Q passive components.

Noise Figure – Small signal amplifiers such as LNA's used in satellite receiver applications require capacitors that exhibit high Q. Lossy passive components will add to thermal (KTB) noise and degrade the overall noise figure of the amplifier thereby reducing the signal to noise ratio.

Likewise, MRI imaging coils also require extremely low loss capacitors. These applications utilize capacitors for tuning the coil in a resonant circuit, and must be transparent in that application. The signals being detected by MRI coils are sufficiently small that any loss contribution from low Q capacitors would generate increased thermal noise, making it difficult or impossible to process the signal.

Thermal Management – (Refer to Figure 1). In extreme cases, If C_3 is very lossy, it can get hot enough to melt solder due to high circulating currents. This can easily cause components to de-solder from the board as a result of excessive heat build up. Since C_3 is physically close to the active device, any additional heat generated by the capacitor will be reflected into the transistor thereby reducing reliability and possibly causing early device failure. Although it is desirable to mount matching capacitors physically close to the transistor's device plane for optimal RF performance, thermal management must be judiciously accounted for in these applications. Improper selection of capacitors in critical applications can easily lead to a myriad of circuit performance issues.

Example: Consider the following application:

Power Amplifier @ 150 MHZ
Output Power = 400 W.
System Impedance = 50 ohm.
$I = \sqrt{P/Z} = \sqrt{400/50} = 2.83$ A. rms.

Assume that an output coupling capacitor in a 400W amplifier has an ESR of 0.022 ohms. Under this condition power dissipation of the capacitor will be i^2 x ESR or 2.83^2 x 0.022 = 176 milliwatts. In this example we see that the power dissipated by the capacitor is directly related to the ESR, making Hi Q low ESR capacitors quintessential for this application. Even small signal amplifiers that do not generate large currents will suffer in effective gain and overall noise figure if losses are not kept to a minimum.

The following table shows typical power dissipation as a function of ESR at octavely related frequencies. The KYOCERA AVX 100B series, 220pF capacitor is compared to a typical 0805 NPO 220pF.

Frequency (MHz)	ESR (ohm) 100B 220pF	Power Dissipation (W) 100B 220pF	ESR (ohm) Typical 0805 NPO 220pF	Power Dissipation (W) Typical 0805 NPO 220pF
150	0.025	0.200	0.08	0.640
300	0.035	0.280	0.113	0.904
600	0.049	0.392	0.159	1.272
1200	0.069	0.552	0.224	1.792

Reliability – Excessive heat generated by lossy capacitors will affect the reliability of the active device as well as other components associated with or in close proximity to the heat source. Lossy capacitors in coupling, matching, bypass and blocking applications can easily lead to decreased MTBF of the entire circuit.

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