TECHNICAL INFORMATION

FACTORS RESPONSIBLE FOR THERMAL SHOCK BEHAVIOR OF CHIP CAPACITORS

By Bharat S. Rawal,
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Abstract:

Thermal shock behavior of multilayer ceramic chip capacitors was evaluated for different ceramic dielectrics with varying construction and design considerations, effects of terminations and role of physical defects to decrease the thermal stresses and decrease failure rates. Parameters such as thermal diffusivity including surface heat transfer coefficient, elastic modulus and thickness of chips are used to explain the results. A secondary goal of this evaluation was to identify the significant wave soldering parameters which could be utilized to eliminate the thermal shock failures of these chips.

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I. Introduction

The study of mechanical properties and thermal shock resistance parameters of multilayer ceramic capacitors (MLCs) is becoming increasingly important because of their increase in surface mount applications. A brief description of various aspects of this complex subject is given in the following paragraphs and some of the important factors are experimentally evaluated in this paper, a first in a series of papers to be devoted to this important subject. The obvious approach appears to be to consider the different sources of stresses possible in these devices, and then study the critical stress intensity factors and slow subcritical crack growth to obtain the critical stresses the devices can tolerate above which deleterious flaws result. This will allow us to study various aspects of the surface mount applications.

A. Complexities of the MLC itself:

As described earlier,[1] this monolithic device consists of barium titanate based dielectric ceramics with interleaved layers of palladium or palladium-silver alloys, and a termination which consists of Pd/Ag alloys and/or a nickel barrier and a solder coating. This device is mounted on a substrate with or without epoxy and all these materials have a wide spectrum of thermal expansion coefficients and these are listed in Table 1. Residual stresses

TABLE 1

MATERIAL	CTEs (ppm/°C)
Barium Titanate Based Ceramics	9.5-11.5
Pd/Ag Alloys	13-17
Tin Lead Alloys	27
Nickel	13-14
Copper	17.6
Alumina	7
FR-4/G-10 PCB (in x-y directions only)	18
Polyimide Glass PCB (in x-y directions only)	12
Polyimide Kevlar PCB (in x-y directions only)	7
Epoxy Adhesives	20-100

and other mechanical properties like elastic modulus and hardness have been studied[2] on polished sections of MLCs utilizing fracture mechanics analysis based on the propagation of mutually perpendicular penny-like median/radial cracks using the Vicker's micro-indentation techniques, and by indentation-biaxial fracture techniques for inert strength measurements.[3,4] These residual stresses by themselves are expected[2] to make only a small contribution to the overall stress state in these devices compared to the thermal stresses.

B. Thermal Stresses

When ceramics are subjected to a rapid change in temperature (such as plunging MLCs in a solder bath) stresses result because the surface reaches the new temperature instantly and the interior either remains at the initial temperature or, in most practical cases, there is a temperature gradient. For various geometries with parabolic temperature distributions where the average temperature is intermediate between the surface and center temperature, the corresponding stress σ_s is found to be such that

$$\sigma_s \propto \Delta T \qquad (1)$$

where ΔT is the temperature difference between the surface and center of a sample. This may be rewritten as

$$\sigma_s = \frac{E\alpha}{(1-\mu)} \quad \frac{S\phi t^2}{(k/\rho C_p)} \qquad (2)$$

where E is the elastic modulus, α is the coefficient of linear thermal expansion, s is the shape factor (s is 0.33 for a plate and 0.221 for a cube), ϕ is the rate of change of temperature, t is, for example, the half thickness for a plate, μ is Poisson's ratio and $(k/\rho C_p)$ is the thermal diffusivity with k, ρ and C_p being the thermal conductivity, density and specific heat respectively. It is realized that for an MLC we are really dealing with a composite of metal-ceramic layers, and anisotropy of various parameters listed in equation (2) is expected; these aspects will be discussed in a later paper.[6] As equation (2) suggests and as a number of analytical studies have shown.[7-9] materials with low E, low α and low μ along with high thermal diffusivity are desirable. Equation (2) and these studies also clearly demonstrate that, when comparing materials or processes, lower rates of change of temperature and especially thinner geometries (because of the square dependence on the thickness) are desirable.

Aside from the thermal conductivity k, another parameter which must be considered in heat transfer studies and corresponding thermal stresses in materials, is the surface heat transfer coefficient, h. This parameter changes rapidly with the surface characteristics of materials and it increases with improving contact between the two media across which the heat transfer takes place. Because of a temperature gradient surface stresses result in the material and this stress is proportional to h/k.

Now that the thermal stress has been identified, its effect on crack initiation and crack propagation should be recognized. Both these processes are important for the thermal stress or thermal shock resistance of ceramic materials.

1. Crack Initiation

The effect of thermal stresses on different materials[3,5] depends not only on stress level, stress distribution and stress duration but also on material characteristics such as ductility, homogeneity, porosity and pre-existing flaws. Because of so many characteristics involved in the thermal stress evaluations, it is impossible to define a single thermal stress resistance factor which is satisfactory for various situations.

Most electronic ceramic materials behave like ideal elastic materials which fracture when the surface stress reaches a particular level. For conditions mentioned above the thermal stress resistance factor R' is defined in Equation 3:

$$R' = \frac{k\sigma_f (1-\mu)}{E\alpha} \qquad (3)$$

where σ_f is the fracture stress. This equation suggests that high fracture stress, low modulus of elasticity and low thermal expansion coefficient indicate a good resistance to thermal stress failure. Once again by considering the failure criterion of fracture occurring when the thermal stress reaches the fracture stress, it is possible to estimate the maximum temperature difference which a sample can withstand and this temperature difference is directly proportional to R' and inversely proportional to half sample thickness t and to the surface heat transfer coefficient h.

The above discussion is predicated on the assumption that failure occurs when the thermal stress reaches the fracture stress. It should, however, be noted that this condition is for the nucleation or initiation of cracks only. These stresses may be initiated at a surface but may be stopped by a pore, a heterogeneity or a grain boundary. These features will be qualitatively studied in the experimental section of this paper where various dielectric materials subjected to similar thermal stresses behave quite differently.

2. Crack Propagation

The conditions which govern the propagation of cracks rather than the nucleation are related[8,9] to the elastic energy stored at the moment of fracture. There are two thermal shock resistance parameters[8,9] which are involved in the avoidance of catastrophic crack propagation and they show a direct proportionality to the elastic modulus E, to the surface fracture energy G and inverse dependence to σ_f^2. Thus the favorable material characteristics for crack propagation are high modulus and high surface fracture energy and low fracture strengths, in direct contrast to conditions appropriate for avoiding the initiation of cracks. In most electronic ceramic materials conditions for avoiding crack initiation are emphasized because micro-cracks may have a deleterious effect on other properties like the electrical conductivity. This is in strong contrast to, for example, porous refractory ceramic materials where large stress gradients initiate many surface cracks which are stopped primarily by pores, grain boundaries or metal layers. These stress relief sites are therefore important for high temperature stress corrosion resistance.

C. Critical Fracture Toughness

Critical stresses which the ceramic materials can withstand can be determined by fracture mechanics analysis of micro-indentations based on propagation of mutually perpendicular penny-like median/radial cracks. When an indentation is put on the sample using the Vicker's indenter, the net driving force in the crack system is a result of two superimposed components (an elastic component and a residual component) which are compressive and tensile respectively. The residual component drives the crack to its final size when the indenter is removed and the restraining elastic component results in a well-defined crack which can be measured under an optical microscope. This technique provides a means to determine critical fracture toughness,

$$K_{1_C} \cong 0.013 \left(\frac{E}{H}\right)^{1/2} \left(\frac{P}{C_o^{3/2}}\right) \qquad (4)$$

where H is the Vicker's hardness, P is the applied load and C_o is the equilibrium crack length in an isotropic material measured soon after the indentation. The corresponding critical stress at which a crack is initiated is:

$$\sigma_C = K_{1_C}/y \sqrt{C_o} \qquad (5)$$
$$\text{where } y = 2/\sqrt{\pi}$$

The critical stress may be anisotropic in a MLC because of residual stresses which can be determined by studying the deviation and anisotropy of the measured crack lengths. In the study of slow crack growth, the underlying assumption is that these cracks will propagate when the stress intensity in the crack tip reaches the value corresponding to K_{1_C}. An exponent in describing the crack velocity related to the fracture toughness can be defined[3] and this allows comparison of different dielectric materials. These results will be discussed in a later paper.[6]

II. Experimental Procedure

In an effort to understand the various sources of thermal stresses and corresponding thermal stress resistance characteristics, various experiments were carried out and these are outlined below:

A. Ceramic Formulations

Since different materials show varying susceptibility to similar thermal shock experiments, chips were fabricated using standard capacitor manufacturing techniques[1] with various dielectric compositions classified by EIA temperature characteristics referred to as NP0, X7R and Z5U ceramics. Even within the same temperature characteristic such as an X7R there are various ceramics used and the differences are minor additives referred to as fluxes which change the sintering temperatures of these materials. Various materials used for experiments are listed in Table

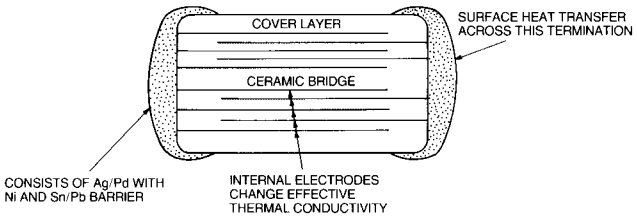
2. Several materials listed in this table are only experimental and are utilized for understanding the thermal shock behavior.

TABLE 2

CERAMIC	TEMP. DESIG.	BASE COMPOSITION	MINOR FLUX ADDITIVES	$K_{1C,}$ CERAMIC
A	NP0	RARE EARTH OXIDE	YES	1.4
B	NP0	MAGNESIUM TITANATE	NO	1.5
C	X7R	BARIUM TITANATE	YES	1.1
D	X7R	BARIUM TITANATE	YES	1.2
E	X7R	BARIUM TITANATE	NO	0.6-0.8
F	Z5U	BARIUM TITANATE	NO	0.85
G	Z5U	BARIUM TITANATE	NO	—

B. Design Considerations

Samples were prepared from ceramics 'A' through 'F' (listed in Table 2) to study the effects of design changes in the 1206 size MLCs. This was done by changing the number and placement of electrode layers while the overall chip thickness was held constant. Both bridged designs,



where the electrode stack is separated by a thick ceramic layer in the middle referred to as a "bridge", and non-bridged designs were utilized to make the chips. MLCs (1206 size) were also made with electrode thicknesses of 3.3μm and 5.5μm by using different screen mesh sizes.

C. Effect of Chip Thickness

Since thermal stresses are known to change as a function of the square of unit thickness and are also dependent on the coefficient of thermal expansion, chips were prepared with varying thicknesses from 0.38mm to 1.52mm for 1206, 1210 and 1812 size chips from ceramic D using non-bridged designs only.

D. Effect of Dielectric Thickness

As mentioned earlier, these devices are really metal-ceramic composites and varying the dielectric thickness should change the effective thermal conductivity and therefore the stress gradients in these chips. This effect was studied by preparing 1210 size chips using ceramic D with constant cover layer and overall thicknesses, but varying dielectric thicknesses from 25 to 229 microns.

E. Effect of Termination

Another technique to change the thermal stresses and stress gradients is to utilize different types of terminations like Pd/Ag alloys or silver which is plated with nickel and a 90Sn/10Pb solder coating. The nickel thickness during the plating process is maintained at 2.0 ± 0.5 microns except for experiments where the effect of plating thickness of Ni was evaluated and the average thickness was varied from 1.5 to 18.4 microns.

F. Role of Flaws

Samples with various flaws like delaminations or cracks identified in chips prepared with ceramic G were tested for thermal shock resistance where thirteen groups with varying degree of flaws were studied.

G. Thermal Stress Resistance and Wave Solder Conditions

Of the four basic soldering processes (hot air reflow, infrared reflow, vapor phase reflow and wave soldering), it appears that wave soldering results in the largest temperature gradients and therefore the largest stress gradients. To simulate this process, two test conditions were utilized to evaluate chips studied in experimental procedures (A) through (F). In the first test condition (known as the solder dip test), chips were picked with metal tweezers along the ceramic edges of the chip and dipped in 60Sn/40Pb solder at 260° and/or 425°C with no preheat such that either of the termination ends enters the solder and the chip is vertical. The tweezer is dipped in chloroethane, VG after each test to keep the tweezer at room temperature. In the second case, the chips were mounted on a board and a wave soldering temperature of 260°C was used. The wave soldering technique was further evaluated and set-up parameters like the preheat and the speed of the board through the preheat and into the solder wave were varied. In all these cases, the chips were visually examined for cracks and these results are reported and discussed below. Several lots were also sectioned and polished to examine differences between external visual cracks and internal cracks and it was found that in general most cracks emerged at the surface. Correlation between various samples considering combined internal and external cracks, and only external cracks were found to be similar in behavior. For this reason, only external cracks were utilized in subsequent experiments. These results are reported and discussed below.

III. Results and Discussion

The various experiments listed above are now discussed in the following paragraphs.

A. Behavior of Ceramic Dielectrics

As indicated earlier, various ceramic dielectric materials behave quite differently under similar thermal shock experiments. Dielectric compositions classified by their temperature coefficients as NP0, X7R and Z5U were utilized to prepare 1206 size chips with various active layers and overall thicknesses of 0.85mm and 1.15mm, respectively. The results of the solder dip test of parts dipped in 60Sn/40Pb solder at 260°C did not show any visual cracks. To study differences in the various ceramic materials, parts with Pd/Ag terminations were dipped in 60Sn/40Pb solder at 425°C with no preheat and the results are shown in Table 3. The results show:

TABLE 3

THERMAL SHOCK STUDIES OF 1206 SIZE CHIPS WITH Pd/Ag TERMINATION

OVERALL CHIP THICKNESS IN MILS (mm)			33 (0.85)							45 (1.15)		
NO. OF ELECTRODES WITH NO BRIDGE			0	2	4	8	16	24	NO COVER LAYERS	0	24	NO COVER LAYERS
CERAMIC	ELECT. THICK. (μm)	GREEN DIELECT. THICK. IN MILS (μm)	SOLDER DIP TEST RESULTS AT 425°C (800°F), NO PREHEAT (Number of units with visual cracks in percent)									
A	3.3	1.6 (41)	0	0	0	0	0	0	0	0	0	0
		3.0 (76)	0	0	0	0	0	0	0	0	0	0
	5.5	1.6 (41)	0	0	0	0	0	0	0	0	0	0
		3.0 (76)	0	0	0	0	0	0	0	0	0	0
B	5.5	3.0 (76)	0	0	0	0	0	0	0	0	0	0
C	3.3	1.6 (41)	0	21	1	1	0	0	0	0	0	3
		2.4 (61)	0	33	2	0	0	0	0	0	0	0
	5.5	1.6 (41)	0	9	0	0	0	0	0	0	0	0
		2.4 (61)	0	6	0	0	0	0	0	0	0	0
D	3.3	1.4 (36)	6	41	20	5	2	0	0	4	3	2
E	3.3	1.4 (36)	0	0	0	3	90	0	0	0	96	3
F	3.3	1.5 (38)	1	0	1	6	12	9	0	0	17	0

1. **NP0 Chips** (Ceramics A and B) have excellent thermal shock resistance with none of the units showing any visual cracks. This is attributed to their relatively higher critical stress intensity factors of about 1.4 $MPam^{1/2}$ which prevents crack initiation and to the two phase pyrochlore microstructure of these materials which slows crack propagation as evidenced by the partial intergranular nature of the fracture along with various crack deflection sites in these ceramics.[3] Ceramic A also has minor additives added as fluxes which form additional grain boundary and other phases which in turn further slow down the crack propagation. These aspects will be discussed further in our next paper.
2. **X7R Materials** (Ceramics C and D) show an anomalous behavior where the ceramic itself exhibits no cracks and parts with high number of electrodes show no visual cracks. However, parts made with 2 to 16 electrodes develop many visual cracks with a 3.3μm electrode thickness, and fewer with a 5.5μm electrode thickness. This behavior is not exhibited by ceramic E in the same table, even though this is an X7R material as well. The behavior of ceramics C and D is characteristic of X7R materials prepared with minor fluxing additives which contain bismuth. Pd is known to diffuse into the ceramic and the remaining electrode is richer in Ag which in turn results in formation of Bi-Ag-Pd based alloys leaving porous electrodes. The corresponding ceramic cavities act as crack initiation sites resulting in thermal shock failures. This problem can be minimized by higher density modified electrodes and practically eliminated by the bridge designs discussed below.
3. **Ceramics E and F** show higher number of visual cracks with high active MLCs. These are attributed to physical flaws which are discussed later.

B. Design Considerations

It was just demonstrated that X7R parts with 2-16 electrodes with no bridge show a significant number of visual cracks. Chips (size 1206) with 2-16 electrodes with a "bridge" are tested under similar conditions and Table 4 shows that NP0 parts once again show excellent thermal shock resistance while X7R parts show a dramatic improvement. The improvement is attributed to the reduction of temperature gradients and corresponding stress gradients in these chips due to a relatively higher effective thermal conductivity near the surface of these chips because of the presence of electrodes. This aspect will be evaluated further in section (D) below.

To evaluate the bridge design further, 1210 X7R 0.1μF parts are tested with and without a bridge and similar overall chip thickness, and these results are shown in Table 5; the parts with a bridge definitely show an improvement with lower number of visual cracks in the solder dip test. The overall chip thickness can be used to further improve the parts and this is discussed in the next section.

TABLE 4

THERMAL SHOCK STUDIES OF 1206 SIZE CHIPS WITH BRIDGE DESIGN AND Pd/Ag TERMINATION

OVERALL CHIP THICKNESS IN MILS (mm)		33 (0.85)				
NO. OF ELECTRODES WITH A BRIDGE		0	2	4	8	16
CERAMIC	GREEN DIELECTRIC THICKNESS IN MILS (μm)	SOLDER DIP TEST RESULTS AT 425°C (800°F), NO PREHEAT (NUMBER OF UNITS WITH VISUAL CRACKS IN PERCENT)				
A	1.6 (41)	0	0	0	0	0
	3.0 (76)	0	0	0	0	0
C	1.5 (38)	0	0	0	0	0
	2.4 (61)	0	0	0	0	0

TABLE 5

THERMAL SHOCK STUDIES OF CERAMIC AS AFFECTED BY DESIGN OF CHIP 1210 X7R 0.1μF, PLATED

OVERALL CHIP THICKNESS IN MILS (mm)	33 (0.85)	46 (1.17)	46 (1.17)
	SOLDER DIP TEST RESULTS AT 260°C (500°F), NO PREHEAT		
CHIP DESIGN	25A/35T* NO BRIDGE	25A/48T BRIDGE DESIGN	25A/48T NO BRIDGE
LOT #			
1	6	21	63
2	5	15	22
3	7	13	31
4	12	18	30
5	2	11	20
X =	6.4	15.6	33.2

*A STANDS FOR ACTIVE LAYERS, T IS THE TOTAL NUMBER OF CERAMIC LAYERS

C. Effect of Chip Thickness

As discussed in the theoretical section of this paper, thermal stresses depend on the square of the overall chip thickness; therefore, this parameter is very important in the chip design and subsequent thermal shock behavior. The 1210 X7R 0.1μF parts with an overall chip thickness of 1.17mm were redesigned with an overall chip thickness of 0.85mm, and the solder dip test results at 260°C in Table 5 clearly demonstrate that the visual cracks were further reduced by more than half to about 6.4%. This is expected as the thermal stresses are reduced by about 85%.

To evaluate the effect of chip thickness further, various commonly used chip styles were prepared with thicknesses ranging from 0.38mm to 1.52mm.

TABLE 6

EFFECT OF THICKNESS ON THERMAL SHOCK OF CERAMIC D PLATED CHIPS

	OVERALL CHIP THICKNESS IN MILS (mm)					
	15 (0.38)	20 (0.51)	25 (0.64)	30 (0.76)	40 (1.01)	60 (1.52)
CHIP STYLE	SOLDER DIP TEST RESULTS AT 260°C (500°F), NO PREHEAT					
1206	0	0	0	0	2	3
1210	0	0	0	1	2	24
1812	0	0	0	2	11	41

The solder dip test results, shown in Table 6, once again confirm that as the thicknesses increase the number of visual cracks increase. It should be further noted that, in general for thick parts at a constant chip thickness, as the part size increases the visual cracks increase and this is not surprising because larger geometries have larger stresses resulting from thermal mismatch between ceramic and electrode layers for the same temperature change. This information is being utilized to make optimum geometries for similar valued parts by AVX.

D. Effect of Dielectric Thickness

Chips were prepared with constant overall chip and cover layer thicknesses and the ceramic dielectric layer thickness was varied from 25 to 229μm. These results, shown in Table 7, demonstrate that the effective thermal conductivity of the composite increases as the dielectric thickness decreases which in turn decreases the temperature and stress gradients and the corresponding number of visual cracks. This experiment further supports the use of the bridge design for low active parts as a viable alternative.

TABLE 7

THERMAL SHOCK FAILURES AS A FUNCTION OF DIELECTRIC THICKNESS

CERAMIC D, 1210 CHIPS WITH 40 MIL (1.02mm) OVERALL THICKNESS, TERMINATED AND SOLDER PLATED

DIELECTRIC THICKNESS IN MILS (μm)	SOLDER DIP TEST RESULTS AT 260°C (500°F), NO PREHEAT (NUMBER OF UNITS WITH VISUAL CRACKS IN PERCENT)
1.0 (25)	2
2.0 (51)	17
3.0 (76)	18
4.0 (101)	16
5.0 (127)	19
9.0 (229)	49

E. Effect of Termination

As indicated earlier, termination materials play a very important role in the thermal shock behavior of MLCs. Chips made with Pd/Ag termination materials and with Ag termination which is subsequently plated with nickel and solder, and then subjected to the solder dip test show dramatic differences. An example of this behavior is shown in Table 8 where 1210 size 0.1μF chips made with ceramic D show no visual cracks with Pd/Ag terminations but the same parts with Ag termination which is plated with about 2.0μm of nickel and 4.0μm of solder show cracks in practically 100% of the parts.

TABLE 8

ROLE OF TERMINATION IN THERMAL SHOCK STUDIES

1210 CHIPS 0.1 μF CERAMIC C, 61 MILS (1.55mm) OVERALL THICKNESS					
	Pd/Ag Termination	Ag termination with Ni Barrier and solder plated	Ni Barrier parts, no solder	Ni Barrier parts heat treated to 160°C for 1 hr.	Ni Barrier parts heat treated at 400°C for 1 hr.
Solder dip test results at 260°C, no preheat (number of units with visual cracks to total parts tested)	0/200	199/200	100/100	70/100	0/100

These observations may be explained by the following analysis.

Thermal conductivity data for Pd/Ag alloys or termination materials is not available but some estimates can be generated. Pd and Ag have thermal conductivity values of about 84 and 428 $Wm^{-1}° K^{-1}$ respectively.[10] Typical Pd/Ag alloys are therefore expected to have values of around 200 $Wm^{-1}° K^{-1}$. However, most termination materials have glass frits added to improve adhesion of these materials to the MLC. Without going into the details of proprietary glass frit materials used for terminations, and utilizing average values of thermal conductivity for glasses of about 0.84 $Wm^{-1}° K^{-1}$ along with the assumption that these glass frits form a grain boundary phase or are at the ceramic-termination interface, the effective thermal conductivity can be calculated[11] to be somewhere between 10 to 25 $Wm^{-1}° K^{-1}$. No provision has been made for a small amount of porosity which may exist in the termination as the thermal conductivity of pores[11] is around 0.02 $Wm^{-1}° K^{-1}$ and these values are expected to be lowered further to about 6-20 $Wm^{-1}° K^{-1}$. In contrast the nickel barrier is dense and nickel has a thermal conductivity of about 84 $Wm^{-1}° K^{-1}$ which is about an order of magnitude higher. Aside from the differences in the thermal conductivities, it was observed during the solder dipping experiments that (even though both the Pd/Ag and plated barrier layer terminations wet well), the plated terminations wet much faster compared to the Pd/Ag terminated chips. This in turn implies that the surface heat transfer coefficient for the plated terminations is significantly higher compared to that for Pd/Ag parts. This nickel layer therefore transfers the heat at the termination rapidly resulting in larger stress gradients compared to parts with Pd/Ag termination only and these stress gradients result in 100% visual cracks in the solder dip test. To further illustrate the validity of this hypothesis, chips with a nickel barrier but no protective solder coating (customarily used) were oxidized at 160° and at 400°C respectively for 1 hour; solder dip test results are shown in Table 8. The results show a dramatic drop in the number of visual cracks after the solder dip test and this is attributed to an order of magnitude lower thermal conductivity of nickel oxide and to a significantly lower surface heat transfer coefficient of an oxide film. This demonstrates the importance of the role of the termination itself. The termination geometry has also been found to be a very important parameter which in turn controls the surface heat transfer coefficient and the subsequent visual cracks due to stress gradients. These aspects are utilized to control the thermal shock behavior of chips and will be discussed in the next paper.[6]

To study the effect of the plating thickness on the termination, chips with various plating thicknesses as characterized by the plating time were tested and the results are shown in Table 9. For 1812 size chips, the actual plated nickel thicknesses are shown in brackets. The results clearly show that at Ni thicknesses above 4.8μm failures in the solder dip test increase and these may be attributed to either stresses due to the differential thermal expansions of nickel and the chip or to residual stresses. This phenomenon is not clearly understood at this time.

TABLE 9

THERMAL SHOCK STUDIES VS. BARRIER LAYER THICKNESS FOR CERAMIC D

			PLATING TIME (MIN.)				
			7.5	15	30	60	120
CHIP STYLE	DESIGN (ACTIVES/ TOTAL)	OVERALL CHIP THICKNESS IN MILS (IN MM)	SOLDER DIP TEST RESULTS AT 260°C (500°F), NO PREHEAT (NUMBER OF UNITS WITH VISUAL CRACKS TO TOTAL PARTS STUDIED)				
1206	24/43	44 (1.12)	1/50	0/50	0/50	0/50	2/50
1210	32/49	61 (1.55)	0/50	3/50	2/50	5/50	5/50
1812	32/39	40 (1.02)	1/50 80* (2.03)	1/50 160* (4.13)	0/50 190* (4.80)	5/50 340* (8.70)	5/50 725* (18.41)

*ACTUAL NI BARRIER LAYER THICKNESS IN MICROINCHES (MICRONS)

F. Role of Flaws

In Table 3, parts made with ceramic E and F with high number of active layers were found to show higher number of visual cracks after the solder dip test and these are attributed to numerous physical flaws in these parts. To investigate the effect of physical flaws, chips made with ceramic G were tested. In this case, parts were processed through various sintering conditions for a completely different series of evaluations; the corresponding flaws generated are listed in Table 10.

TABLE 10

THERMAL SHOCK BEHAVIOR AS AFFECTED BY PHYSICAL FLAWS OF CERAMIC G

ALL UNITS WITH PD/AG TERMINATIONS

	TYPES OF FLAW (% OF UNITS WITH FLAWS)		SOLDER DIP TEST RESULTS AT 425°C, NO PREHEAT (NUMBER OF UNITS WITH VISUAL CRACKS AS %)	
GROUP #	External Delaminations	External Cracks	External Delaminations	
1	71	2	100	100
2	44	-	85	95
3	84	-	82	90
4	18	-	40	86
5	77	-	87	86
6	37	-	49	81
7	20	-	42	81
8	49	-	76	76
9	5	15	7	76
10*	-	-	-	52
11	40	-	9	48
12	-	-	-	5

*THIS GROUP HAS POROUS ELECTRODES WHICH MAY ACT AS SITES FOR CRACK INITIATION

There is only a general correlation between number of flaws and the solder dip test results. These flaws act as crack initiation sites. Results of group 10 were at first misleading because apparently no flaws were found; however, closer examination revealed porous electrodes which have already been shown to act as sites for crack initiation.

G. Soldering Considerations

As indicated earlier, wave soldering was often used as a test vehicle to simulate the temperature and/or stress gradients in the chips studied. Two important parameters studied were the preheat temperature and the immersion rate of the part into the solder. Immersion rate was preferred over the actual temperature rise for the chips because it was impossible to read the temperature change accurately; this can be done by burying the thermocouple in the part, and the results of these experiments will be reported at a later date. The immersion rate is determined by the belt speed carrying the boards into the wave; a common rate of 1.22 m/min. is used in the industry.

The results of these experiments are shown in Table 11 where it is clearly seen that both the preheat and the immersion rate are critical to controlling the soldering process. Our recommendation is that the preheat temperature as measured on the board should be a maximum of 100°C below the temperature of the wave and the rate of immersion should be 1.2 m/min. Results in Table 11 show how these results may be optimized but since different ceramic materials show varying degrees of thermal shock susceptibility, the recommended conditions should be followed wherever possible.

TABLE 11

ROLE OF WAVE SOLDER PARAMETERS WITH WAVE TEMPERATURE OF 260°C (500°F) OF CERAMIC D

ALL CHIPS ARE PLATED

		BOARD TEST RESULTS (NUMBER OF UNITS WITH VISUAL CRACKS TO TOTAL UNITS TESTED)	
SOLDER CONDITIONS		GROUP A	GROUP B
PREHEAT, IF ANY (°C)	BELT SPEED IN FT/MIN (m/min)	1210, 01μF, 25A/48T WITH BRIDGE, 45 MILS THICK	1210, 01μF, 25A/35T, NO BRIDGE, 33 MILS THICK
NONE	4 (1.2)	9/240	3/240
	20 (6.1)	51/240	6/240
NONE	4 (1.2)	8/240	1/240
	20 (6.1)	41/240	2/240
NONE	4 (1.2)	0/240	0/240
	10 (3.0)	15/240	1/240
	20 (6.1)	26/240	2/240

Conclusions

1. Chips made from NP0 dielectric materials show excellent thermal shock behavior in surface mount applications.
2. Chips made with 2-12 active layers from X7R dielectrics with bismuth containing additives may exhibit thermal shock failures if the electrodes are porous. This problem may be minimized with denser electrodes and with bridge designs.
3. Bridge designs can dramatically improve thermal shock behavior exhibited by chips made with X7R dielectrics.
4. Thickness of the chip plays a very important role in the overall chip design and visual cracks can be dramatically reduced with the decrease in overall chip thickness.

5. As the dielectric thickness increases, the susceptibility to thermal shock may increase for X7R dielectrics. This result supports the utilization of the bridge design as a viable technique to improve thermal shock behavior.
6. Nickel barrier terminations show higher susceptibility to thermal shock compared to Pd/Ag terminated chips. The termination geometry becomes an important parameter and it may be used to reduce these failures; this will be discussed in the next paper.
7. There is a general correlation between physical flaws and thermal shock susceptibility of chips. Physical flaws such as major delaminations and porous electrodes act as crack initiation sites.
8. Both the preheat temperature and the immersion rate are very important in wave soldering techniques. A preheat temperature as measured on the board should be a maximum of 100°C below the temperature of the wave. A 1.2 m/min. immersion is recommended.

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